PATENT
8006-1026

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Hidefumi NATSUME et al. Conf. 6372

Application No. 10/700,451 Group 2619

Filed November 5, 2003 Examiner R. Abelson

LAYER 2 SWITCH AND METHOD OF PROCESSING
EXPANSION VLAN TAG OF LAYER 2 FRAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed Form PTO-1449.

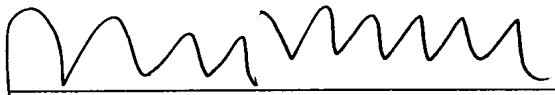
A concise explanation of the relevance of these items is that these references were cited by the Japanese Patent Office in an Official Action. A copy of the Japanese Official Action in which they were cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. **An English translation of the enclosed portion is also attached hereto.**

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a

counterpart foreign application not more than three months prior to the filing of this Statement.

Respectfully submitted,

YOUNG & THOMPSON



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